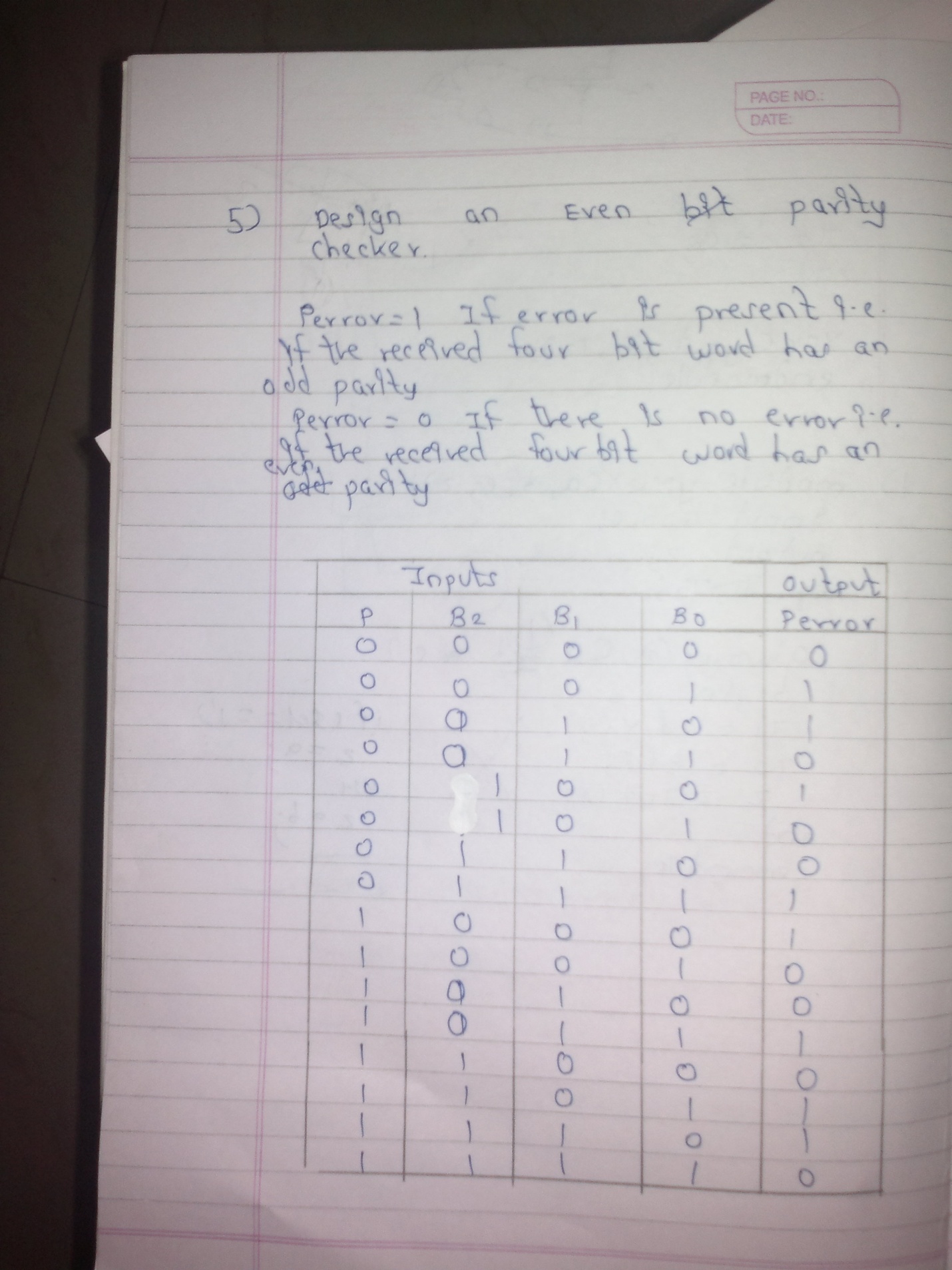
**Homework assignment Q.no 5)**

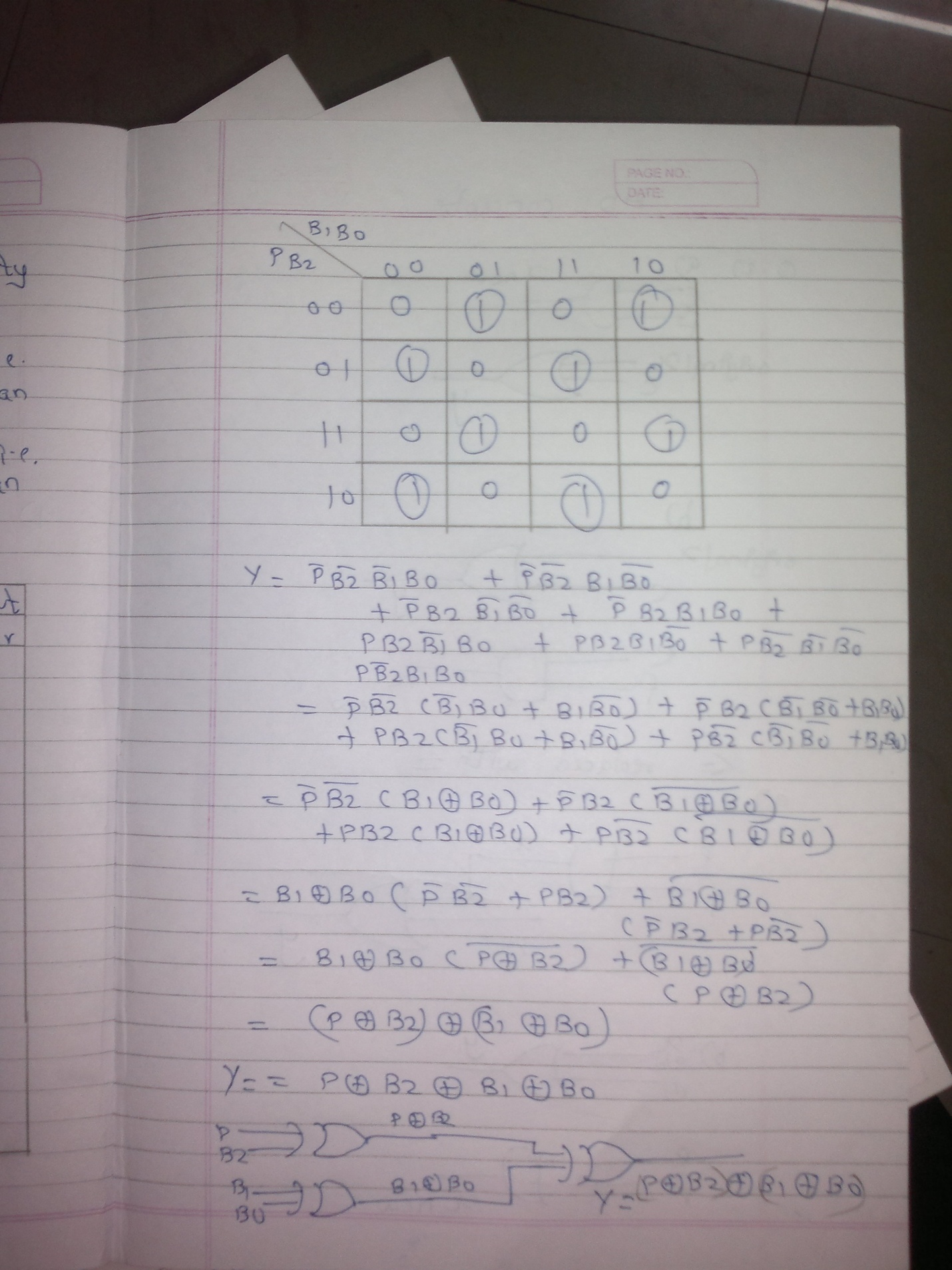
**1)Understanding the Problem:**

In the above program we have to design a 4 bit parity checker which should follow even parity. The received word with parity bit is applied to the parity checker which will check parity and give op.

**2) Devising a Plan/Design:**

Here we want to design a 4 bit parity checker.So it will be 3 data bits & one parity bit. We will use Dataflow programming for the execution.





1. **Carrying out the plan:**

**Verilog code:**

module parity(

input p,

input B2,

input B1,

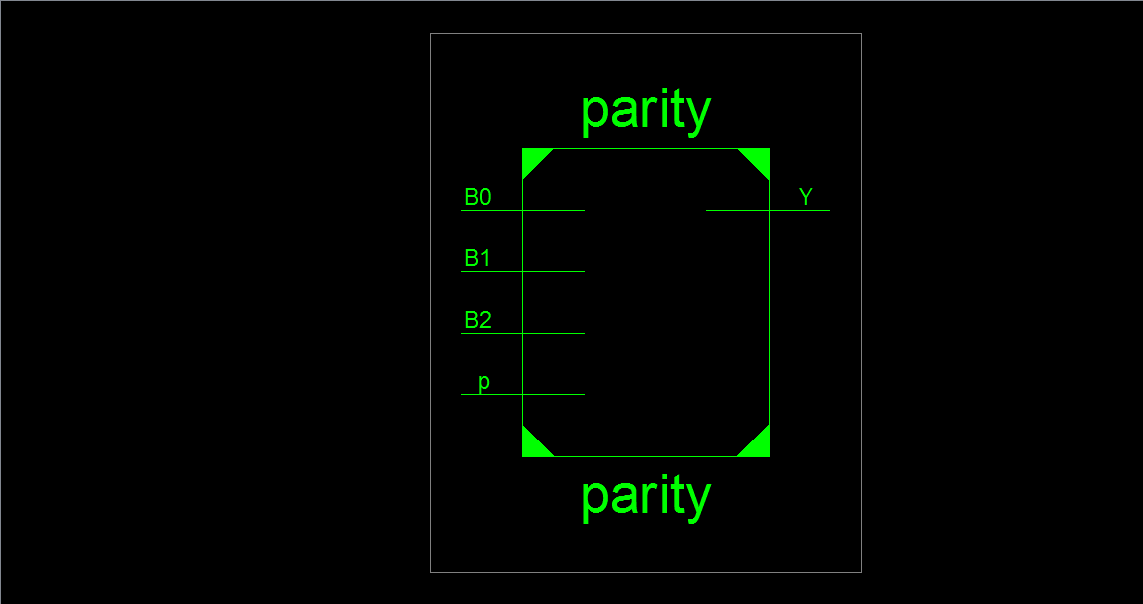
input B0,

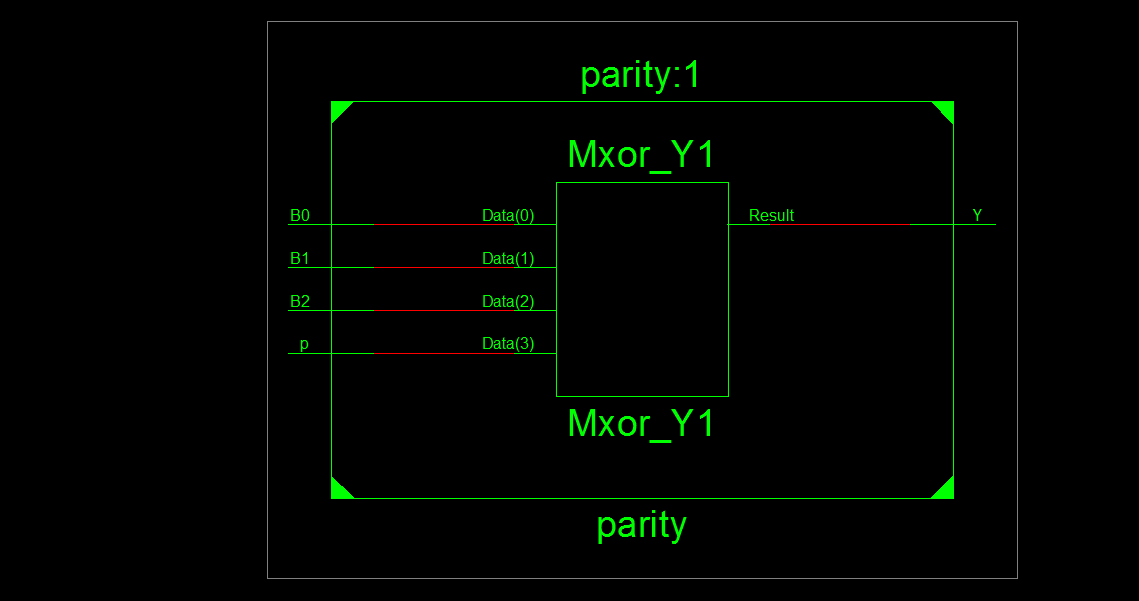
output Y

);

assign Y=(p^B2)^(B1^B0);

endmodule





**Testbench:**

module parity\_tb;

// Inputs

reg p;

reg B2;

reg B1;

reg B0;

// Outputs

wire Y;

// Instantiate the Unit Under Test (UUT)

parity uut (

.p(p),

.B2(B2),

.B1(B1),

.B0(B0),

.Y(Y)

);

initial begin

// Initialize Inputs

p = 0;

B2 = 0;

B1 = 0;

B0 = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

p=1'b1;

B2=1'b1;

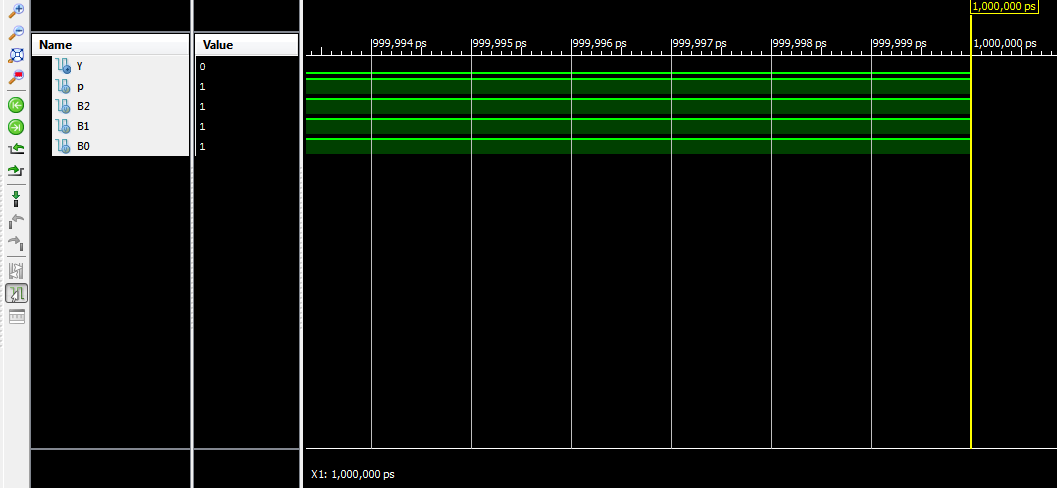
B1=1'b1;

B0=1'b1;

#100;

end

endmodule



**4)Looking back/Self reflection:**

In the above program we implemented 4 bit parity checker with even parity.It is used in communication circuits for checking the parity of received data. The same program could have been executed by behavioural programming.

***Synthesis report:***

Release 12.1 - xst M.53d (nt)

Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Reading design: parity.prj

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6.1) Advanced HDL Synthesis Report

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8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "parity.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "parity"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : parity

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : parity.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling verilog file "parity.v" in library work

Module <parity> compiled

No errors in compilation

Analysis of file <"parity.prj"> succeeded.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for module <parity> in library <work>.

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing top module <parity>.

Module <parity> is correct for synthesis.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <parity>.

Related source file is "parity.v".

Found 1-bit xor4 for signal <Y>.

Summary:

inferred 1 Xor(s).

Unit <parity> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Xors : 1

1-bit xor4 : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Xors : 1

1-bit xor4 : 1

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <parity> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block parity, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Found no macro

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : parity.ngr

Top Level Output File Name : parity

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 5

Cell Usage :

# BELS : 1

# LUT4 : 1

# IO Buffers : 5

# IBUF : 4

# OBUF : 1

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 3s200pq208-5

Number of Slices: 1 out of 1920 0%

Number of 4 input LUTs: 1 out of 3840 0%

Number of IOs: 5

Number of bonded IOBs: 5 out of 141 3%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

No clock signals found in this design

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 7.760ns

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 4 / 1

-------------------------------------------------------------------------

Delay: 7.760ns (Levels of Logic = 3)

Source: B1 (PAD)

Destination: Y (PAD)

Data Path: B1 to Y

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 1 0.715 0.976 B1\_IBUF (B1\_IBUF)

LUT4:I0->O 1 0.479 0.681 Mxor\_Y\_xo<0>1 (Y\_OBUF)

OBUF:I->O 4.909 Y\_OBUF (Y)

----------------------------------------

Total 7.760ns (6.103ns logic, 1.657ns route)

(78.6% logic, 21.4% route)

=========================================================================

Total REAL time to Xst completion: 5.00 secs

Total CPU time to Xst completion: 5.54 secs

-->

Total memory usage is 185528 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)